IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Wilk *et al.*	Docket:	TI-24742
Serial No.:	09/176,422	Examiner:	N. Berezny
Filed:	10/21/98	Art Unit:	2823
For:	Low Temperature Method for Forming a Thin, Uniform Oxide		

APPEAL BRIEF TRANSMITTAL FORM

February 28, 2001

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on

March 12, 2001.

Tina Rendon

Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith in triplicate is an Appeal Brief in the above-identified application.

Please charge any required fee for filing the Brief to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **Three copies of this sheet are enclosed.**

Respectfully submitted,

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#11 Appeal Brief Appeal 4/2/01

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APPEAL BRIEF

Applicants' Appeal Brief is submitted pursuant to 37 C.F.R. §1.192 and subsequent to a Notice of Appeal filed February 28, 2001.

Applicants appeal the Examiner's rejection dated December 6, 2000, rejecting claims 1-25.

Real Party In Interest:

This application is assigned to Texas Instruments Incorporated.

Related Appeals And Interferences:

There are no related appeals or interferences.

Status of the Claims on Appeal

Claims 1-25 are pending and rejected.

Status of Amendments Filed After Final Rejection

Applicants filed a response after the final rejection. That response did not change any claims. Examiner considered the response.

Summary of the Invention

This invention pertains generally to forming thin oxides at low temperatures, and more particularly to forming thin oxides with high thickness uniformly. [1:22][1]

Process control of the growth of a 2 nm film requires unprecedented thickness control. At these thicknesses direct tunneling through the SiO2 may occur, although the effect of tunneling current on device performance may not preclude operation. Since the tunnel current depends exponentially on the dielectric thickness, small variations in process control may result in large variations in the tunnel current, possibly leading to reliability problems. [2:24 - 2:31].

Another area of concern is the interface between the gate oxide and the channel region of the substrate. This silicon dioxide/silicon interface should be very flat and uniform to help limit interface scattering of electrons in the channel region.

Rapid thermal oxidation and furnace annealing are two current methods for forming gate oxides. However, current methods do not reliably produce gate oxides with the thickness uniformity and interface smoothness that will be needed to make devices with approximately 1.5 nm, 2 nm, or 2.5 nm gate oxides practical.

We disclose a low temperature method for forming a thin gate oxide on a silicon surface. This method comprises providing a partially completed integrated circuit on a semiconductor substrate with a clean silicon surface; and stabilizing the substrate at a first temperature. The method further includes exposing the silicon surface to an atmosphere containing ozone, while maintaining the substrate at the first temperature. In this method, the exposing step creates a first, uniformly thick, gate oxide film.

Preferably, exposing the silicon surface to an atmosphere containing ozone includes exposing the silicon surface to an atmosphere containing molecular oxygen, while irradiating at least a portion of the atmosphere with ultraviolet light, where the light transforms some of the oxygen to ozone. In some embodiments, the atmosphere further includes an inert gas, such as argon. Preferably, the ozone at the silicon surface is not in an excited energy state, such as a plasma. However, a plasma kept away from the wafer may be more acceptable. [3:1 - 3:28].

[1] [1:22] denotes page 1, line 22.

In some embodiments, the clean silicon surface is atomically flat. Typically, the semiconductor substrate contains some areas that already have some structure, such as a field oxide. In some embodiments, the substrate has a plurality of clean, atomically flat, silicon surfaces. This might occur when the gate oxide is applied to surfaces exposed by etching "windows" in a layer overlying a silicon surface; or when overlying layers are added to the silicon surface, except where "islands" have been masked off. [4:1 - 4:9].

Issues Presented for Review

1. Whether claim 18 is rendered obvious under 35 U.S.C. § 103 by the Fujishiro *et al.* patent (Fujishiro '571) in combination with the Nayar *et al.* article in ELECTRONIC LETTERS (Nayar article).

2. Whether claims 24 and 25 are rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, further in view of the Wolf text, Vol. 3, p. 422-423 (Wolf text).

3. Whether Claims 1 - 13 are rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, in view of the Choquette *et al.* patent (Choquette '687).

4. Whether Claim 23 is rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, in view of Choquette '687, and further , in view of the Wolf text.

Grouping of Claims

Claims 1 - 5 and 7 - 17 stand and fall together. Claims 18 - 22 stand and fall together. Claims 24 - 25 stand and fall together. Claims 6 and 23 each stand independently.

Arguments

Fujishiro '571 and the Nayar article do not render claim 18 obvious

Ordinary artisans would not have a reasonable expectation of success

A. Claim 18's limitations include—among others—"exposing the silicon surface to an atmosphere including ozone, while maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, **gate oxide** film".

The Nayar article teaches a method of growing oxide layers. However, these oxides were not used as gate oxides. The article notes that the fixed oxide charges are high[2], and that the typical breakdown field is approximately 4 MV/cm[3]. The Office Action implied that the GATE OXIDE CHARACTERISTICS NEEDED FOR SUBMICRON MOSFETS section of the Wolf text lists characteristics that ordinary artisans would understand are necessary for/inherent in a conventional MOSFET gate oxide. Three of these characteristics are:

> 2. The specified oxide thickness must also be sufficiently uniform across the entire wafer, and from wafer to wafer, and from run-to-run.
>
> 3. The gate oxide film and the Si/SiO_2 interface must exhibit adequately small values of charge in the oxide and at the $Si-SiO_2$ interface. (i.e., low Q_f, D_{it}, Q_{ot} and Q_m values - see chap. 3).
>
> 4. The dielectric breakdown strength of the oxide must be sufficiently high (e.g., >8 MV/cm), implying that the film is pinhole free and contains a negligible number of defects that would lead to oxide breakdown at lower electric fields.[4]

The Nayar article explicitly teaches that its oxides have high fixed charges. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article explicitly teaches that its oxides breakdown near 4 MV/cm. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article does not mention that the oxide is highly uniform. Instead, the article mentions that the thickness measurements are averages. Additionally, an examination of the Nayar article fig. 2 shows that at 250° C, the oxide thickness may not be well behaved. Ordinary artisans would not be assured that the Nayar article oxides had sufficient thickness uniformity for a conventional gate oxide.

In short, Applicants submit that an ordinary artisans would not consider an approach based on the Nayar article to have a reasonable expectation of success.[5] Without this expectation of success, obviousness has not been shown.

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[2] Nayar article, [206:first full paragraph].
[3] *id.*
[4] Wolf text, [422].
[5] "Obviousness does not require absolute predictability, but a reasonable expectation of success is necessary." -- In Re Clinton, 188 U.S.P.Q. 365 (CCPA, 1976).

The postulated combination does not teach how to achieve a critical limitation of the claim

B. Applicants' claim 18 limitations also include the requirement that the gate oxide be uniformly thick. Nayar's useful method of forming extremely thick oxide layers at low temperatures makes no mention of obtaining uniform thicknesses. Instead, the Nayar article states that the thickness data is an average of several measurements[6]. Applicants submit that if Nayar had found high thickness uniformity (such as Applicants' <3% uniformity), the Nayar article would have reported the achievement. However, there is no evidence that the Nayar article's useful method creates uniformly thick layers—to which Applicants' claims are limited.

As Applicants understand it, the Office Action submits that uniformly thick layers would be an inherent property of a gate oxide. This may often be true. However, the Nayar article does not form gate oxides. Instead, it forms oxide films that are not suitable for use as gate oxides[7]. Applicants submit that uniform thickness is not an inherent property of an ordinary oxide. Thus, there is no evidence that the cited references teach how to achieve a critical limitation of the claim.

Applicants submit that the claims are patentable over the cited references because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 18 and its dependants.

Fujishiro '571, the Nayar article, and the Wolf text do not render claims 24 and 25 obvious

C. Applicants arguments for claim 18 above are equally applicable to claims 24 and 25, and are repeated here by reference.

Applicants note that the Office Action alleges that these claims do not further limit the scope of claim 18. Applicants disagree with this objection. Claim 24 is exemplary. Claim 24 further limits claim 18, in that it limits the types of methods of forming thin gate oxides on silicon surfaces that would infringe this claim. Applicants submit that a process—that used the steps in the claim—to make a gate oxide with a breakdown strength of 8 MV/cm would infringe claim 18, but not infringe claim 24.

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[6] Nayar article [206:3].
[7] See argument A, *supra*.

The postulated combination does not teach how to achieve a critical limitation of the claims

D. Claims 24 and 25 are further limited to methods that create gate oxide films with breakdown voltages greater than 10 MV/cm or 12 MV/cm. The Nayar article that was cited as a similar process does not teach a method capable of forming gate oxide films with these breakdown voltages. The other cited references do not seem to cure this deficiency either.

Applicants submit that the claims are patentable over the cited references because of their dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claims 24 and 25.

Fujishiro '571, the Nayar article, and Choquette '687 do not render claim 1 obvious

E. Applicants arguments for claim 18 above are equally applicable to claim 1, and are repeated here by reference.

Ordinary artisans would not reasonably expect Choquette '687's GaAs process to produce the claimed atomically flat, silicon surface

F. Claim 1's limitations also include "providing a partially completed integrated circuit on a semiconductor substrate with a clean, **atomically flat, silicon surface**". Choquette '687 teaches a useful process for removing surface contaminants such as C, Si and O, from substrates of the gallium arsenide or indium phosphide families. Applicants have studied Choquette '687—including the abstract section cited—and have not found where it teaches a method of forming an atomically flat Si surface. The abstract does mention that this method forms an atomically smooth semiconductor surface. However, when read in context with the rest of the disclosure, Applicants submit that Choquette '687 enables forming atomically smooth surfaces on III-IV semiconductors, such as gallium arsenide, indium phosphide, and the like. Applicants submit that ordinary artisans would not reasonably expect a method to remove Si from a GaAs surface would be useful to form the claimed atomically flat, silicon surface. As such, obviousness has not been established.

Applicants also disagree with Examiner's assertion that ordinary artisans would be clearly motivated to provide an atomically flat surface. The cited references do not indicate that

this type of surface is required. In the absence of a need for an atomically flat surface, ordinary artisans would be motivated to eliminate unnecessary steps in order to reduce costs.

Applicants submit that the claims are patentable over the cited references because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 1 and its dependents.

Fujishiro '571, the Nayar article, and Choquette '687 do not render claim 6 obvious

G. Claim 6 is dependant upon claim 1, and is allowable since the base claim is allowable. However claim 6 has additional limitations not taught or suggested by the cited art. These limitations include "exposing the silicon surface to an atmosphere with less energy than a plasma", and wherein "at least part of the atmosphere that does not contact the silicon surface includes an ozone plasma."

Applicants do not see where the cited art teaches or suggests using a remote ozone plasma. Instead, the Nayar article teaches a UV/ozone method to oxidize silicon.

Applicants submit that claim 6 is are patentable over the cited references because of it dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claim 6.

Fujishiro '571, the Nayar article, Choquette '687, and the Wolf text do not render claim 23 obvious

H. Applicants arguments for claims 18, 24, and 1 above are equally applicable to claim 23 and are repeated here—in combination—by reference.

Applicants submit that claim 23 is are patentable over the cited references because of it dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claim 23.

Conclusion

Claim 18 and its dependants are patentable over Fujishiro '571 and the Nayar article. Ordinary artisans would not have a reasonable expectation of success since the Nayar article teaches oxides that do not have characteristics that ordinary artisans look for in a conventional gate dielectric. Additionally, there is no evidence that the postulated combination achieves a critical limitation of the claim—that the gate oxide be uniformly thick.

Claims 24 and 25 are patentable over Fujishiro '571, the Nayar article, and the Wolf text. The postulated combination does not teach how to achieve another critical limitation of the claims—that the method create gate oxide films with breakdown voltages greater than 10 MV/cm or 12 MV/cm.

Claim 1 and its dependants are patentable over Fujishiro '571, the Nayar article, and Choquette '687. The arguments for claim 18 above are equally applicable to claim 1, and ordinary artisans would not reasonably expect Choquette '687's GaAs process to produce the claimed atomically flat, silicon surface.

Fujishiro '571, the Nayar article, and Choquette '687 do not render claim 6 obvious. Claim 6 is dependant upon an allowable base claim, and the cited art does not teach or suggest a remote ozone plasma.

Applicants believe that the application is in condition for allowance. However, should the honorable Board have any comments or suggestions, Applicant respectfully requests that the honorable Board contact the undersigned in order to quickly resolve any outstanding issues.

Please charge any required fee to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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